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EXAMINER	
RAMPURIA, SATISH	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,482	CHEN ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/9/06 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the Amendment filed on Jan 9, 2006.

2. The Oat/Declaration was found with the Transmittal letter filed on Oct. 23, 2002, as pointed out by the Applicants.

3. The objection to drawing (Fig. 1 and 4) is withdrawn in view of applicant's replacement drawings.

4. The objection to claims 1-20 is withdrawn in view of Applicant's amendment.

5. The rejections under 35 U.S.C. §112 second paragraph to claim 1-20 is withdrawn in view of applicant's amendment.

6. Claims amended by the Applicant: 1 and 11.

7. Claims pending in the application: 1-20.

Response to Arguments

8. Applicant's arguments with respect to claims have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

(i) The applicant would like to point out how independent claims 1 and 11 are not obvious over claims 9 and 1 in the '043 patent. '043 patent fails to teach that the value of the program counter of the microprocessor should be changed after updating the firmware and the microprocessor executing the program code stored in the firmware memory at a predetermined location of the program code instead of

executing a next instruction in the program code located after the current position of the program counter.

(ii) '043 patent fails to teach that the value of the program counter of the microprocessor should be changed after updating the firmware and the microprocessor executing the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter. For these reasons, the applicant submits that independent claims 1 and 11 are patentable over the teachings of the '043 patent.

Examiner's response:

(i) In response to Applicant's argument, '043 does not explicitly discloses the value of the program counter of the microprocessor should be changed after updating the firmware and the microprocessor executing the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter. However, the feature of changing or resetting the program counter to execute the program stored at the predetermined location is inherent to '043 system. The independent claims 1 and 11 would be obvious over claims 9 and 1 in the '043 patent. Therefore, the double patenting rejection is proper and maintained herein.

(ii) In response to Applicant's argument, the response to argument (i) applies here as well since the arguments are same.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 9, 10, 11, 19 and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9, 11, 12, 1, 2 and 3 of U. S. Patent No.

6,170,043 to Hu (hereinafter called '043). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observation.

Instant Claim	*'043 Claim*
1. **An update method used in an optical disk system to update firmware information, which is stored in a firmware memory, using a microprocessor, wherein the firmware memory serves as an intrinsic execution program memory, the method comprising** steps: **fetching** a program code and **an update program** routine **from an update source**;	9. **An update method used in an optic-disk system to update its firmware information, which is stored in a firmware memory, through a microprocessor, wherein the firmware memory serves as an intrinsic execution program memory, the method comprising**: **fetching an update program** with a characteristic format **from a compact disk (CD)**, in which the update program includes a program code and an update program routine;
storing the program code into a first buffer memory, and storing the update program routine into a second buffer memory, wherein the microprocessor accesses the firmware memory as a data access memory, and accesses the second buffer memory as an execution program memory;	**storing the program code into a first buffer memory, and the update program routine into a second buffer memory, wherein the microprocessor accesses to the second buffer memory at a special address, treats the firmware memory as a data access memory, and treats the second buffer memory as an**

executing the update program routine stored in the second buffer memory, and using the update program routine to **write the program code stored in the first buffer memory into the firmware memory in order to update the firmware information; accessing the firmware memory as intrinsic execution program memory, and accessing the second buffer memory as intrinsic data access memory;** changing a value of a program counter of the microprocessor such that the microprocessor executes the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter; **and using the program code as updated firmware information to control the optical disk system.**	**execution program memory; executing the update program routine stored in the second buffer memory; writing the program code stored in the first buffer memory into the firmware memory to update the firmware information; treating the firmware memory back as its intrinsic execution program memory, and treating the second buffer memory back as its intrinsic data access memory;** **and using the program code as an updated firmware information to control the opticdisk system and provide any kind of updated information residing in the program code.**

9. The method of claim 1, **wherein the firmware memory is a flash memory.**	11. The method of claim 9, **wherein the firmware memory comprises a flash memory.**
10. The method of claim 1, **wherein the firmware memory is an electrically erasable programmable read only memory (EEPROM).**	12. The method of claim 9, **wherein the firmware memory comprises an electrical erasable programmable read only memory (EEPROM).**
11. **An optical disk system control chip, used in an optical disk system to update firmware information, the control chip comprising:** **a microprocessor, coupled to a data bus, wherein the microprocessor is also coupled to a firmware memory through the data bus, in which the firmware memory is used to store the firmware information;** **a decoder, coupled to the microprocessor through the data bus, wherein the decoder is also coupled to a first buffer memory,** and the decoder receives updated firmware information from an update source; **a controller, coupled to the decoder, and**	1. **An optic-disk system control chip, used in an optic-disk system to update its firmware information, the control chip comprising:** **a microprocessor, coupled to a data bus, wherein the microprocessor is also coupled to an external memory through the data bus, in which the external memory is used to store the firmware information;** **a decoder, coupled to the microprocessor through the data bus, wherein the decoder is also coupled to an external buffer memory,** and an external main board inter face, which serves as an interface to communicate with an external computer; **a controller, coupled to the decoder, and**

coupled to the microprocessor through the data bus, wherein the controller is used to receive a control signal and general data; and	**coupled to the microprocessor through the data bus, wherein the controller is used to receive a control signal and general data; and**
a second buffer memory, coupled to the microprocessor through the data bus, wherein when the optical disk system is operated in an update mode, the microprocessor accesses the firmware memory as a data access memory and accesses the second buffer memory as an execution program memory, and	**an extra memory, coupled to the microprocessor through the data bus, wherein when the optic-disk system is operated at an update mode,** the microprocessor yields at least an output enable signal, a chip selection signal, and a writing-in signal so as to temporarily treat the external memory to as a data access memory and treat the extra memory as an execution program memory, and
after the firmware is completely updated, the second buffer memory is accessed as data access memory and the firmware memory is accessed as execution program memory, and a value of a program counter of the microprocessor is changed such that the microprocessor executes program code stored	**after the firmware is completely updated, the extra memory is treated back as its original data access memory and the external memory is treated back as its original execution program memory.**

in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter.	
19. The control chip of claim 11, **wherein the firmware memory is a flash memory.**	2. The control chip of claim 1, **wherein the external memory comprises a flash memory.**
20. The control chip of claim 11, **wherein the firmware memory is an electrically erasable programmable read only memory (EEPROM).**	3. The control chip of claim 1, **wherein the external memory comprises an electrical erasable programmable read only memory (EEPROM).**

Although, '043 discloses updating the firmware on a device. '043 is silent on changing a value of a program counter of the microprocessor such that the microprocessor executes the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter. However, the feature of changing or resetting the program counter to execute the program stored at the predetermined location deemed to be inherent to '043 system. '043 disclose resetting the microprocessor by turning ON/OFF to initialize the microprocessor (col. 3-4, lines 58-67 and 1-8 and FIG. 3A and FIG. 5 and related discussion). '043 system would in inoperative if microprocessor does not reset to have the new changes in effect.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 6,170,043 to Hu (hereinafter called '043).

Per claim 1:

'043 discloses:

- An update method used in an optical disk system to update firmware information, which is stored in a firmware memory, using a microprocessor, wherein the firmware memory serves as an intrinsic execution program memory (FIG. 7 and related discussion), the method comprising steps:
- fetching a program code and an update program routine from an update source (col. 6, lines 1-4 "the update program routine stored in the second buffer memory is executed to program the data access memory space with the new program code data, in which the data access memory space is the flash memory of FIG. 2 that is the original execution program memory space");
- storing the program code into a first buffer memory (col. 5, lines 51-52 "program code data are stored in a first buffer memory"), and storing the update program routine into a second buffer memory (col. 5, lines 52-53 "and the update program routine is stored in a

second buffer memory"), wherein the microprocessor accesses the firmware memory as a data access memory, and accesses the second buffer memory as an execution program memory (col. 5, lines 62-67 "original execution program memory space is treated as a data access memory space to store the program code data that are to be updated, and the second buffer memory is treated as an execution program memory space to store the update program routine");

- executing the update program routine stored in the second buffer memory, and using the update program routine to write the program code stored in the first buffer memory into the firmware memory in order to update the firmware information (col. 6, lines 1-6 "update program routine stored in the second buffer memory is executed to program the data access memory space with the new program code data, in which the data access memory space is the flash memory of FIG. 2 that is the original execution program memory space");
- accessing the firmware memory as intrinsic execution program memory, and accessing the second buffer memory as intrinsic data access memory (col. 5, lines 62-67 "original execution program memory space is treated as a data access memory space to store the program code data that are to be updated, and the second buffer memory is treated as an execution program memory space to store the update program routine");
- using the program code as updated firmware information to control the optical disk system (col. 6, lines 24-26 "the updated program code data are stored in the flash memory 210 and is to serve as the new firmware information").

Although, '043 discloses updating the firmware on a device. '043 is silent on changing a value of a program counter of the microprocessor such that the microprocessor executes the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter. However, the feature of changing or resetting the program counter to execute the program stored at the predetermined location deemed to be inherent to '043 system. '043 disclose resetting the microprocessor by turning ON/OFF to initialize the microprocessor (col. 3-4, lines 58-67 and 1-8 and FIG. 3A and FIG. 5 and related discussion). '043 system would in inoperative if microprocessor does not reset to have the new changes in effect.

Per claim 2:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein changing the value of the program counter of the microprocessor is performed by resetting the microprocessor, which will reset the program counter of the microprocessor to a predetermined value (FIG. 6 and related discussion).

Per claim 3:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein changing the program counter of the microprocessor is performed by executing a jump statement in the program code of the updated firmware information, and the jump statement will reset the program counter of the microprocessor to a predetermined value (col. 5, lines 1-6 "FIG. 5, after the program code data are downloaded into the buffer

memory 212 and the update program routine is downloaded into the extra memory 202, the microprocessor 204 will jump to a special address, such as the F880h of FIG. 3B, which is determined by the extra memory 202").

Per claim 4:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein the update source, which the program code is fetched from, is an optical disk read by the optical disk system, and the update program routine is fetched from the optical disk read by the optical disk system or from original contents of the flash memory (FIG. 7 and related discussion).

Per claim 5:

The rejection of claim 4 is incorporated, and further, '043 discloses:

- wherein the optical disk is a compact disk, and the optical disk system is a compact disk drive (FIG. 7 and related discussion).

Per claim 6:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein the update source, which the program code is fetched from, is a peripheral device connected to the optical disk system through an interface connection, and the update program routine is fetched from the peripheral device connected to the optical disk system through the interface connection or from original contents of the flash memory

(FIG. 7 and related discussion).

Per claim 7:

The rejection of claim 6 is incorporated, and further, '043 discloses:

- wherein the peripheral device is a computer, onto which the program code and the update program routine have been downloaded from a software source (FIG. 2 and 7 and related discussion).

Per claim 8:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein the interface connection is an IDE interface, an EIDE interface, a SCSI interface, an RS232 interface, a USB interface, or an IEEE 1394 interface (col. 6, lines 34-36 "The update program code can be pre-downloaded into the computer through the main board interface 214 to fetch the desired update program code from a remote data source. The main board interface 214 includes, for example, an IDE interface, enhanced-IDE interface, or a SCSI interface, all of which are common products in the computer market").

Per claim 9:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein the firmware memory is a flash memory (col. 3, lines 23-25 "update firmware information, which is stored in a memory 210, such as a flash memory 210 or an

electrical erasable programmable ROM (EEPROM)").

Per claim 10:

The rejection of claim 1 is incorporated, and further, '043 discloses:

- wherein the firmware memory is an electrically erasable programmable read only memory (EEPROM) (col. 3, lines 23-25 "update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)").

Per claim 11:

'043 discloses:

- An optical disk system control chip, used in an optical disk system to update firmware information (col. 1, lines 61-62 "a CD-ROM control chip is provided for a use of firmware information update"), the control chip comprising:
- a microprocessor, coupled to a data bus, wherein the microprocessor is also coupled to a firmware memory through the data bus, in which the firmware memory is used to store the firmware information (col. 1, lines 62-65 "CD-ROM control chip at least includes a microprocessor, a decoder, a controller, and an extra memory. The microprocessor is coupled to a data bus, and further coupled to an external ROM, which stores all firmware information. The decoder is coupled to the microprocessor through the data bus, and is also coupled to an external buffer memory and an external main board interface");

- a decoder, coupled to the microprocessor through the data bus (col. 1, lines 65-66 "The decoder is coupled to the microprocessor through the data bus"), wherein the decoder is also coupled to a first buffer memory (col. 1, lines 66-67 "and is also coupled to an external buffer memory and an external main board interface"), and the decoder receives updated firmware information from an update source (col. 1, lines 61-62 "a CD-ROM control chip is provided for a use of firmware information update");
- a controller, coupled to the decoder, and coupled to the microprocessor through the data bus, wherein the controller is used to receive a control signal and general data (col. 2, lines 3-7 "The controller is coupled to the decoder, and is coupled to the microprocessor the data bus. The controller is used to receive information and control signals from an external CD"); and
- a second buffer memory, coupled to the microprocessor through the data bus (col. 2, lines 6-7 "The extra memory is coupled to the microprocessor through the data bus "), wherein when the optical disk system is operated in an update mode, the microprocessor accesses the firmware memory as a data access memory and accesses the second buffer memory as an execution program memory (col. 5, lines 62-67 "original execution program memory space is treated as a data access memory space to store the program code data that are to be updated, and the second buffer memory is treated as an execution program memory space to store the update program routine"), and after the firmware is completely updated, the second buffer memory is accessed as data access memory and the firmware memory is accessed as execution program memory (col. 6, lines 1-6 "update program routine stored in the second buffer memory is executed to program the data access

memory space with the new program code data, in which the data access memory space is the flash memory of FIG. 2 that is the original execution program memory space"), and.

Although, '043 discloses updating the firmware on a device. '043 is silent on changing a value of a program counter of the microprocessor such that the microprocessor executes the program code stored in the firmware memory at a predetermined location of the program code instead of executing a next instruction in the program code located after the current position of the program counter. However, the feature of changing or resetting the program counter to execute the program stored at the predetermined location deemed to be inherent to '043 system. '043 disclose resetting the microprocessor by turning ON/OFF to initialize the microprocessor (col. 3-4, lines 58-67 and 1-8 and FIG. 3A and FIG. 5 and related discussion). '043 system would in inoperative if microprocessor does not reset to have the new changes in effect.

Per claim 12:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein the control chip further comprises a control circuit used for generating a reset signal, and changing the value of the program counter of the microprocessor is performed by the control circuit issuing the reset signal to the microprocessor, which will reset the program counter of the microprocessor to a predetermined value (FIG. 6 and related discussion).

Per claim 13:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein changing the program counter of the microprocessor is performed by executing a jump statement in the program code of the updated firmware information, and the jump statement will reset the program counter of the microprocessor to a predetermined value (col. 5, lines 1-6 "FIG. 5, after the program code data are downloaded into the buffer memory 212 and the update program routine is downloaded into the extra memory 202, the microprocessor 204 will jump to a special address, such as the F880h of FIG. 3B, which is determined by the extra memory 202").

Per claim 14:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein the update source, which the updated firmware information is fetched from, is an optical disk read by the optical disk system (FIG. 7 and related discussion).

Per claim 15:

The rejection of claim 14 is incorporated, and further, '043 discloses:

- wherein the optical disk is a compact disk, and the optical disk system is a compact disk drive (FIG. 7 and related discussion).

Per claim 16:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein the update source, which the updated firmware information is fetched from, is a peripheral device connected to the optical disk system through an interface connection(FIG. 2 and 7 and related discussion).

Per claim 17:

The rejection of claim 16 is incorporated, and further, '043 discloses:

- wherein the peripheral device is a computer, onto which the program code and the update program routine have been downloaded from a software source (FIG. 2 and 7 and related discussion).

Per claim 18:

The rejection of claim 16 is incorporated, and further, '043 discloses:

- wherein the interface connection is an IDE interface, an EIDE interface, a SCSI interface, an RS232 interface, a USB interface, or an IEEE 1394 interface (col. 6, lines 34-36 "The update program code can be pre-downloaded into the computer through the main board interface 214 to fetch the desired update program code from a remote data source. The main board interface 214 includes, for example, an IDE interface, enhanced-IDE interface, or a SCSI interface, all of which are common products in the computer market").

Per claim 19:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein the firmware memory is a flash memory (col. 3, lines 23-25 "update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)").

Per claim 20:

The rejection of claim 11 is incorporated, and further, '043 discloses:

- wherein the firmware memory is an electrically erasable programmable read only memory (EEPROM) (col. 3, lines 23-25 "update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)").

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
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Art Unit 2191

WEI ZHEN
SUPERVISORY PATENT EXAMINER